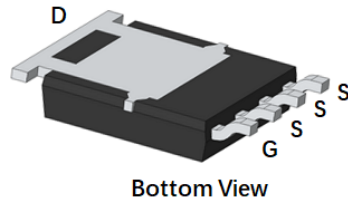
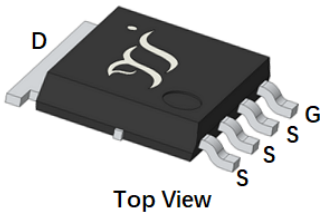
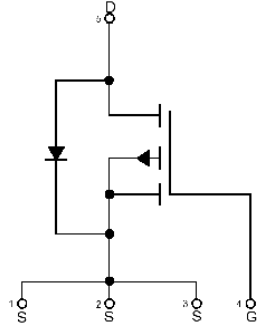


P-Channel Enhancement Mode Field Effect Transistor



LFPAK56W-8L



Product Summary

- V_{DS} -60V
- I_D -70A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <15m Ω
- 100% EAS Tested
- 100% ∇V_{DS} Tested
- ESD Level(HBM) H1C

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

Limiting Values

| Parameter | Conditions | | Symbol | Min | Max | Unit | | |
|--|---|--|----------|----------------|-------|------|------|------------------|
| Drain-source Voltage | | | V_{DS} | - | -60 | V | | |
| Gate-source Voltage (Note 4) | | | V_{GS} | -20 | 20 | | | |
| Continuous Drain Current (Note 1,2) | Steady-State | $T_A=25^\circ\text{C}, V_{GS}=-10\text{V}$ | I_D | - | -9.5 | A | | |
| | | $T_A=100^\circ\text{C}, V_{GS}=-10\text{V}$ | | - | -6.7 | | | |
| Continuous Drain Current (Note 1,3) | Steady-State | $T_C=25^\circ\text{C}, V_{GS}=-10\text{V}, \text{Chip limitation}$ | | - | -70 | | | |
| | | $T_C=100^\circ\text{C}, V_{GS}=-10\text{V}$ | | - | -49.5 | | | |
| Pulsed Drain Current | $T_C=25^\circ\text{C}, t_p \leq 10\mu\text{s}$ | | | I_{DM} | - | | -250 | |
| Maximum Body-Diode Continuous Current | $T_C=25^\circ\text{C}$ | | | I_S | - | | -70 | |
| Avalanche Energy (non-repetitive) | $T_J=25^\circ\text{C}, V_G=-10\text{V}, R_G=25\Omega, L=0.5\text{mH}, I_{AS}=-28\text{A}$ | | EAS | - | 196 | mJ | | |
| Total Power Dissipation (Note 1,2) | Steady-State | $T_A=25^\circ\text{C}$ | P_D | - | 2.6 | W | | |
| | | $T_A=100^\circ\text{C}$ | | - | 1.3 | | | |
| Total Power Dissipation (Note 1,3) | Steady-State | $T_C=25^\circ\text{C}$ | | - | 151 | | | |
| | | $T_C=100^\circ\text{C}$ | | - | 75 | | | |
| Junction and Storage Temperature Range | | | | T_J, T_{STG} | -55 | | 175 | $^\circ\text{C}$ |

Thermal Resistance

| Parameter | | Symbol | Typ | Max | Units |
|---|--------------|-----------------|-----|------|--------------------|
| Thermal Resistance Junction-to-Ambient (Note 2) | Steady-State | $R_{\theta JA}$ | - | 55.9 | $^\circ\text{C/W}$ |
| Thermal Resistance Junction-to-Case | Steady-State | $R_{\theta JC}$ | - | 0.99 | |

Ordering Information (Example)

| PREFERRED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|----------------|--------------|------------|----------------------|-------------------------|----------------------------|---------------|
| YJYA015GP06AHQ | F1 | YA015GP06A | 5000 | 10000 | 100000 | 13" reel |



YJYA015GP06AHQ

■ Electrical Characteristics

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-----------------------------------|--------------|---|------|------|-----------|------------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0V, I_D=-250\mu A, T_j=25^\circ C$ | -60 | - | - | V |
| | | $V_{GS}=0V, I_D=-1mA, T_j=25^\circ C$ | -60 | - | - | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=-60V, V_{GS}=0V, T_j=25^\circ C$ | - | - | -1 | μA |
| | | $V_{DS}=-60V, V_{GS}=0V, T_j=125^\circ C$ | - | - | -100 | |
| Gate-Source Leakage Current | I_{GSS} | $V_{GS}=\pm 20V, V_{DS}=0V, T_j=25^\circ C$ | - | - | ± 100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=-250\mu A, T_j=25^\circ C$ | -1.5 | -2.3 | -3.1 | V |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}=-10V, I_D=-35A, T_j=25^\circ C$ | - | 11 | 15 | m Ω |
| Diode Forward Voltage | V_{SD} | $I_S=-35A, V_{GS}=0V, T_j=25^\circ C$ | - | -0.9 | -1.2 | V |
| Gate Resistance | R_G | $f=1MHz, T_j=25^\circ C$ | - | 1.8 | - | Ω |
| Dynamic Parameters | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS}=-30V, V_{GS}=0V, f=1MHz, T_j=25^\circ C$ | - | 3290 | - | pF |
| Output Capacitance | C_{oss} | | - | 520 | - | |
| Reverse Transfer Capacitance | C_{rss} | | - | 24 | - | |
| Switching Parameters | | | | | | |
| Total Gate Charge | Q_g | $V_{GS}=-10V, V_{DS}=-30V, I_D=-35A, T_j=25^\circ C$ | - | 55.6 | - | nC |
| Gate-Source Charge | Q_{gs} | | - | 10.4 | - | |
| Gate-Drain Charge | Q_{gd} | | - | 10.7 | - | |
| Reverse Recovery Charge | Q_{rr} | $I_F=-35A, di/dt=100A/\mu s, V_{GS}=0V, V_R=-30V, T_j=25^\circ C$ | - | 75.6 | - | nC |
| Reverse Recovery Time | t_{rr} | | - | 43.7 | - | ns |
| Turn-on Delay Time | $t_{D(on)}$ | $V_{GS}=-10V, V_{DS}=-30V, I_D=-35A, R_{GEN}=3\Omega, T_j=25^\circ C$ | - | 15.5 | - | ns |
| Turn-on Rise Time | t_r | | - | 12.3 | - | |
| Turn-off Delay Time | $t_{D(off)}$ | | - | 39.8 | - | |
| Turn-off Fall Time | t_f | | - | 12.6 | - | |

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $175^\circ C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).
- $V_{GS}=-20V/+10V$ according AEC-Q101 at $T_j=175^\circ C$.



Typical Electrical and Thermal Characteristics Diagrams

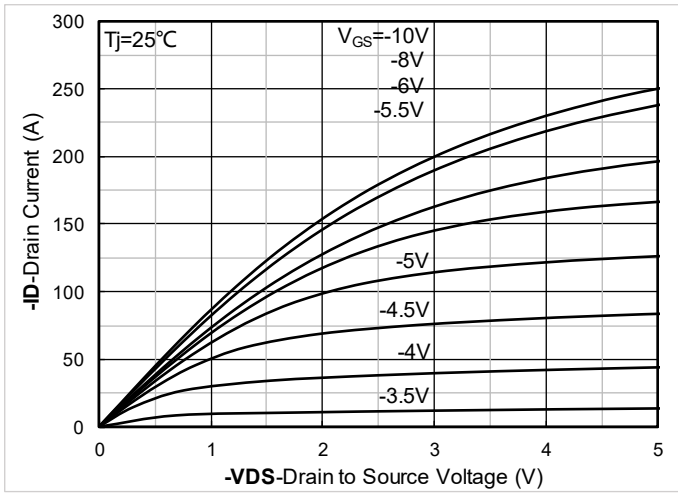


Figure 1. Output Characteristics; typical values

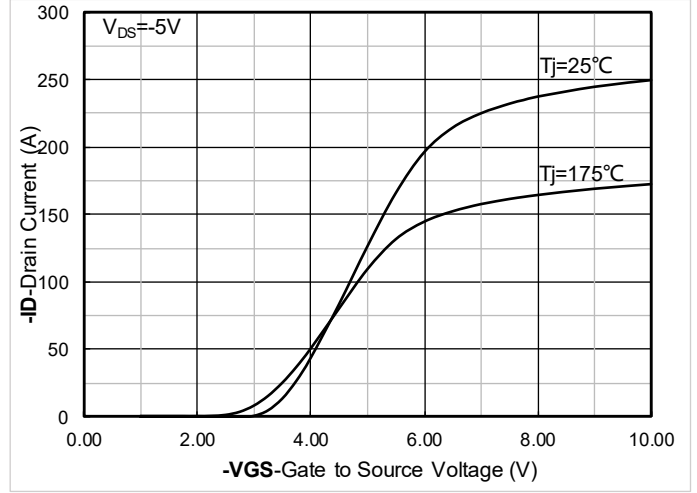


Figure 2. Transfer Characteristics; typical values

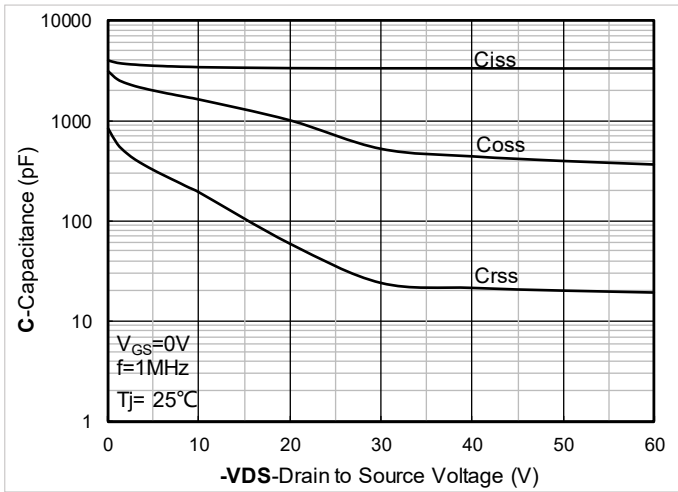


Figure 3. Capacitance Characteristics; typical values

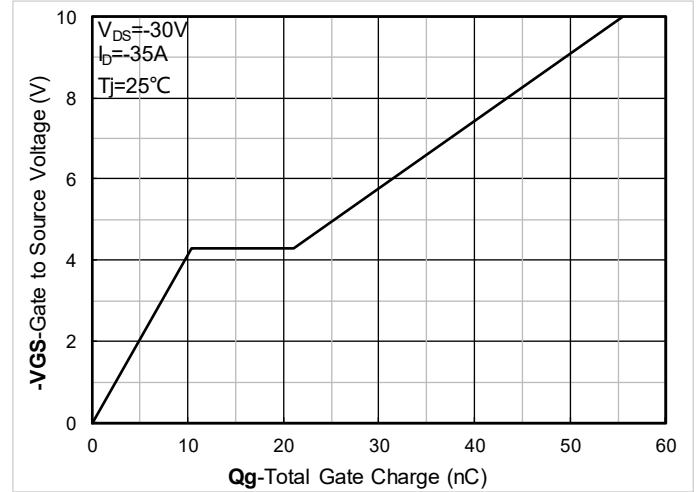


Figure 4. Gate Charge; typical values

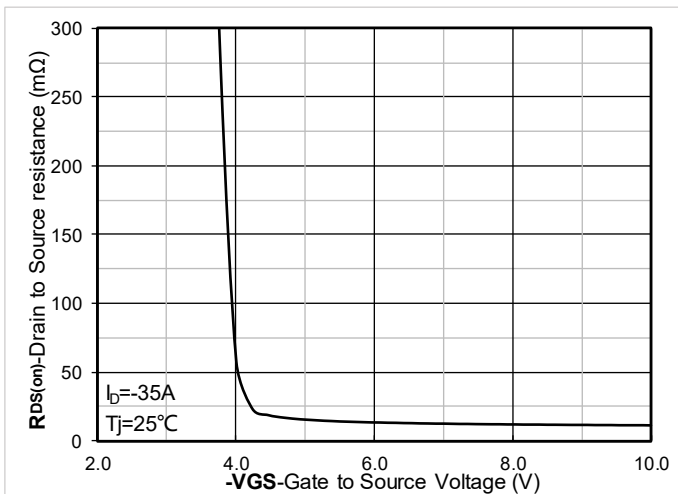


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

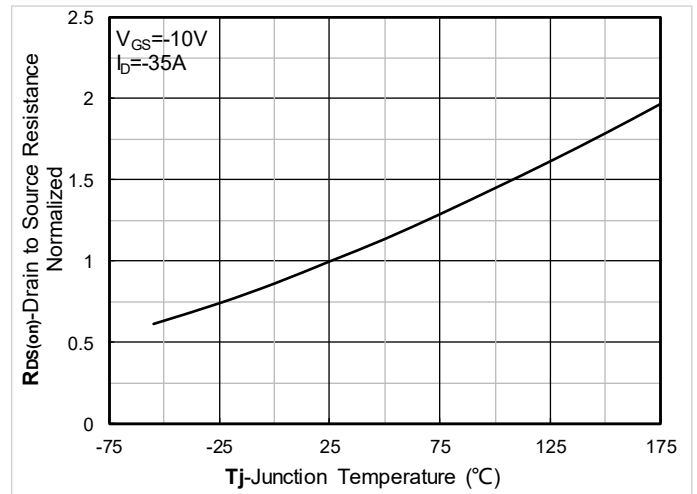


Figure 6. Normalized On-Resistance



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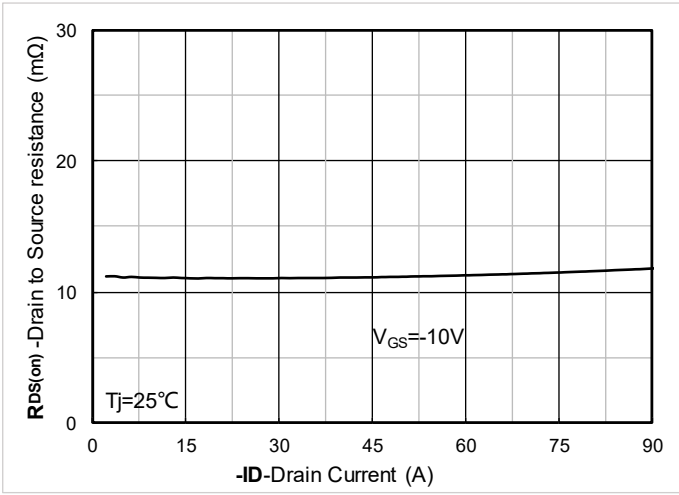


Figure 7. RDS(on) vs. Drain Current; typical values

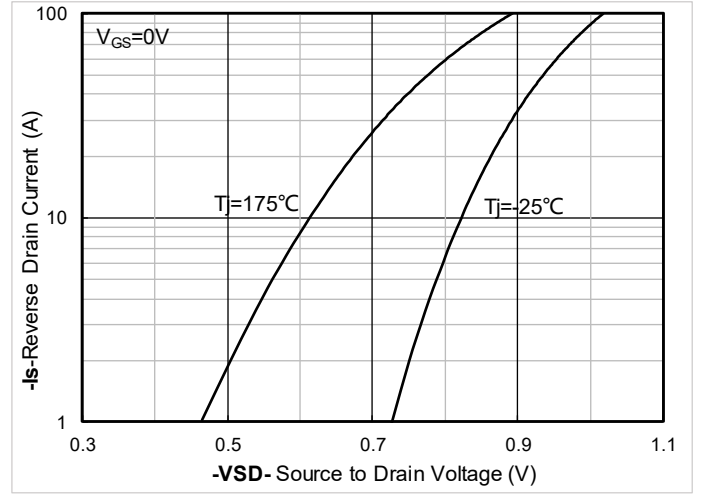


Figure 8. Forward characteristics of reverse diode; typical values

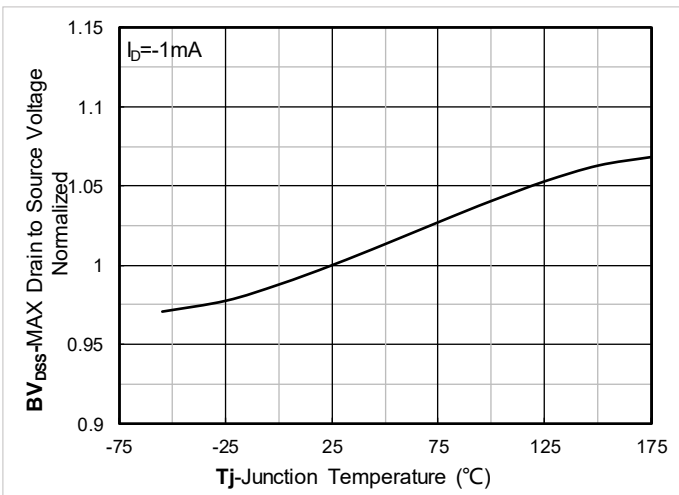


Figure 9. Normalized breakdown voltage

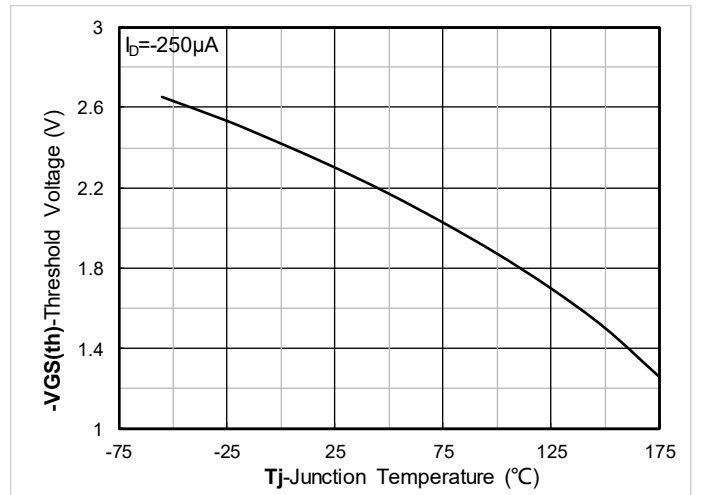


Figure 10. Gate Threshold voltage; typical values

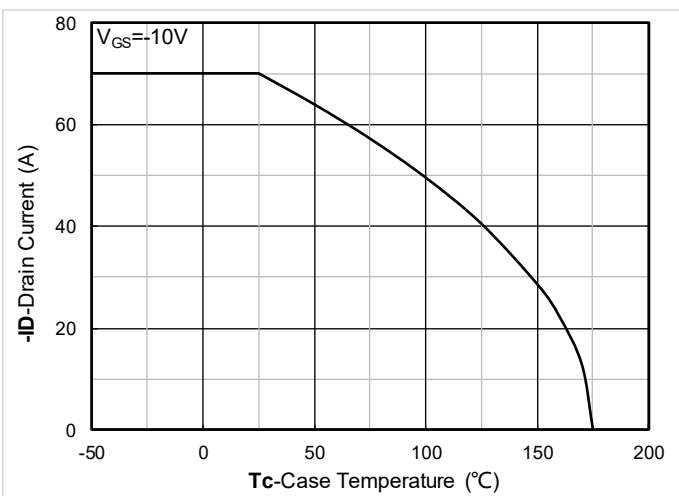


Figure 11. Current dissipation

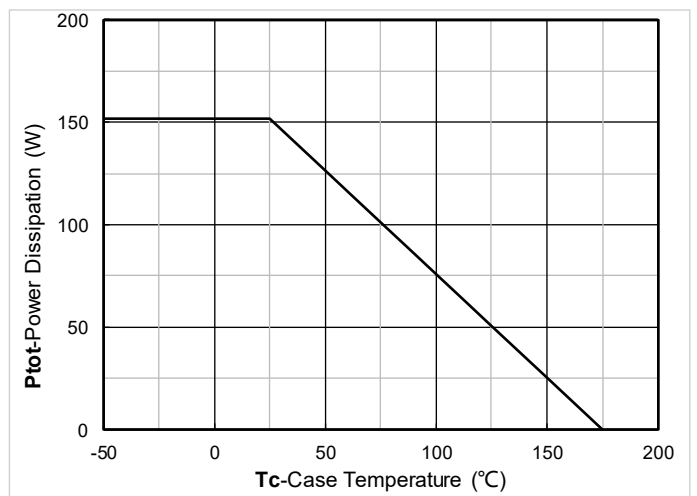


Figure 12. Power dissipation

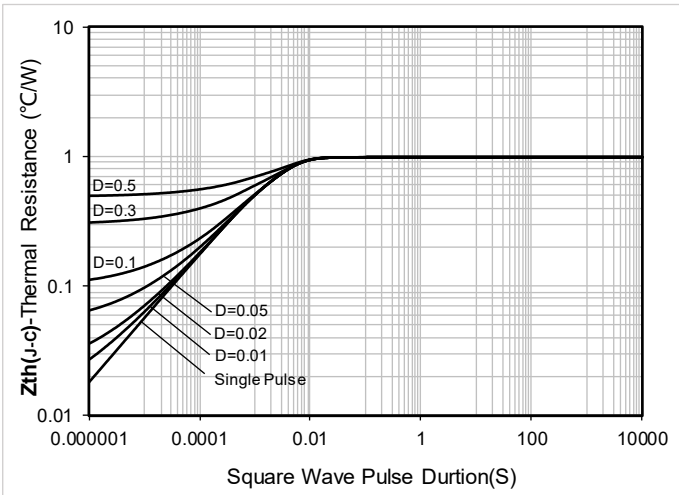


Figure 13. Maximum Transient Thermal Impedance

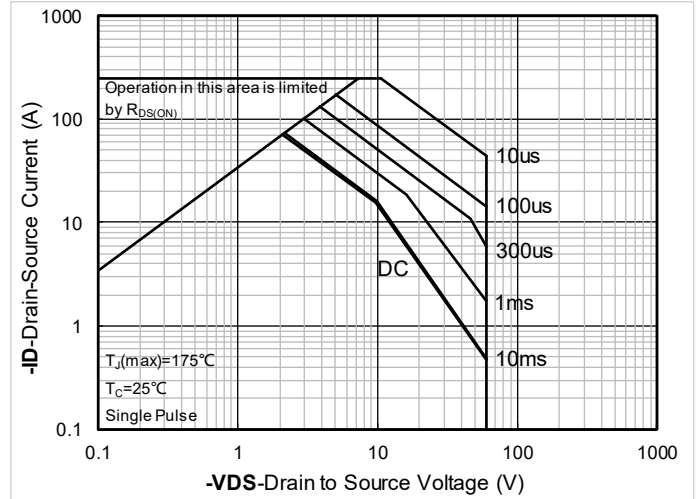
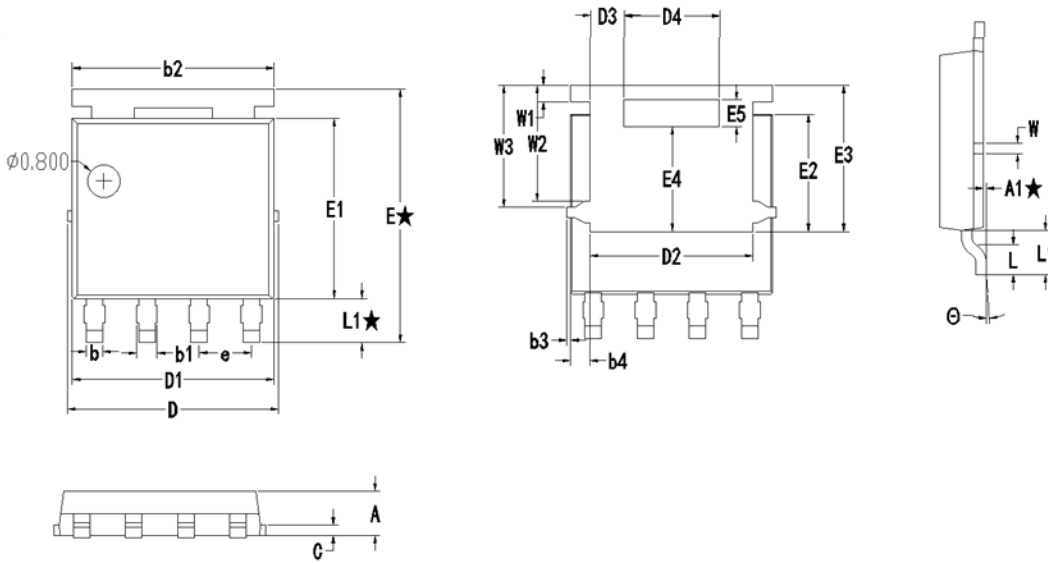


Figure 14. Safe Operation Area



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■ LCPAK56W-8L-A-1.04MM Package information



| SYMBOL | MILLIMETER | | |
|--------|------------|----------|-------|
| | MIN | NOM | MAX |
| A | 1.00 | 1.04 | 1.07 |
| A1 | 0.00 | 0.06 | 0.127 |
| b | 0.33 | 0.41 | 0.48 |
| b1 | 0.44 | 0.51 | 0.58 |
| b2 | 4.80 | 4.90 | 5.00 |
| b3 | - | 0.094 | - |
| b4 | - | 0.47 | - |
| c | 0.20 | 0.254 | 0.30 |
| D | 5.00 | 5.10 | 5.25 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.86 | 3.96 | 4.06 |
| D3 | 0.82 REF | | |
| D4 | 2.32 REF | | |
| E | 6.05 | 6.15 | 6.25 |
| E1 | 4.27 | 4.37 | 4.47 |
| E2 | 2.75 | 2.85 | 2.95 |
| E3 | 3.46 | 3.56 | 3.66 |
| E4 | 2.55 REF | | |
| E5 | 0.65 REF | | |
| e | 1.27 | | |
| L | 0.62 | 0.72 | 0.82 |
| L1 | 0.92 | 1.07 | 1.22 |
| W | - | 0.23 BSC | - |
| W1 | - | 0.41 BSC | - |
| W2 | - | 2.82 BSC | - |
| W3 | - | 2.96 BSC | - |
| θ | 0° | | 10° |

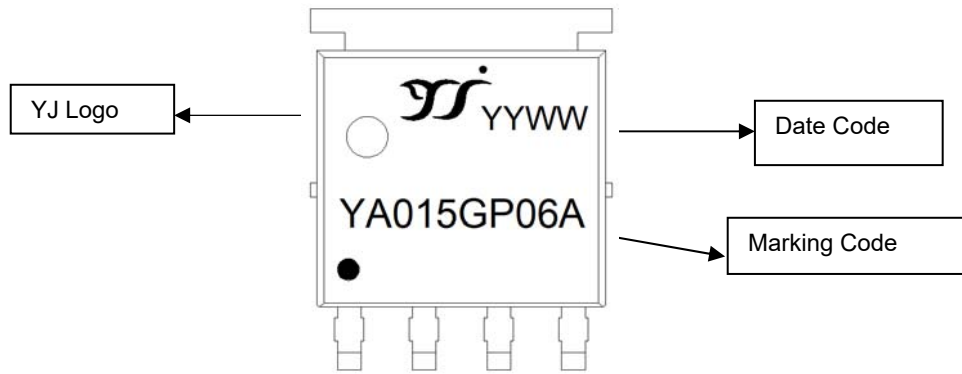
Note:

- All dimensions are in millimeters (mm) unless otherwise specified.
[所有尺寸均以毫米为单位, 除非另有说明]
- General tolerances: $\pm 0.10\text{mm}$ unless otherwise specified.
[通用公差为 $\pm 0.10\text{mm}$, 除非另有说明]
- Dimensions and tolerances per ASME Y14.5M-2018.
[尺寸和公差遵循 ASME Y14.5M-2018 标准]
- All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.
[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]
- Dimension b does not include dambar protrusion of max 0.100 mm per side.
[尺寸b不包括单边最大0.100 MM的中筋凸出部分]
- Dimensions D and E are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.
[D和E是塑封体的外部极限尺寸, 不包括封装溢料、内引线溢料、凸出部分以及胶体毛刺, 但是包含了封装错位的最大尺寸]
- Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.
[成型的管脚应为同一平面, 共面性最大为0.1mm]
- ★It is the key size.
[★ 标记为关键尺寸]



YJYA015GP06AHQ

■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. YA015GP06A is Marking Code., YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



YJYA015GP06AHQ

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